## Remarks/Arguments

Claims 1, 3-6, and 8-9 are pending. Claims 2, 7, and 10 have been cancelled. The claims have been amended to more clearly and distinctly claim the subject matter that applicants regard as their invention. No new matter is believed to be added by the present amendment.

Rejection of claims 1-10 under 35 USC 102(b) as being anticipated by Swenson, et al. (US 5,926,120).

Applicants submit that for the reasons discussed below that current claims 1, 3-6, and 8-9 are not anticipated by Swenson, et al.

The present invention provides a serial compressed bus interface, wherein received serial data is converted to packets of parallel data, and the **packets of parallel data are transferred to an appropriate one of a plurality of devices associated with data applications in response to a signal from an enable logic**.

In the exemplary embodiment, the serial data is received and converted to parallel data by serial to parallel converter 110. The parallel data is transferred to one of the buffers 130-136 in response to the buf_sel signal from enable logic 112. That is, the output of the enable logic 112 identifies which one of the buffers 130-136 are associated with a particular packet of parallel data output from serial to parallel converter 110. Such an arrangement advantageously reduces the pin count required in a serial interface, which receives time-division multiplexed serial data from a plurality of data sources and must transfer each respective data packet to an appropriate data application. In that regard, amended claim 1 recites:

> *a serial-to-parallel converter having a single serial data input line adapted to receive time-division multiplexed serial data from a plurality of data sources, and having a plurality of parallel output lines for* ***providing thereon a packet*** *of said time-division multiplexed serial data in parallel form* ***to one of a plurality of devices associated with data applications****; and*
>
> *enable logic coupled to each of said plurality of devices and adapted to provide at least one* ***data valid signal that identifies which of said plurality of devices is associated with a particular packet*** *of said time-division multiplexed serial data.*

Amended claim 6 recites similar features in method form. Applicants submit that Swenson et al. fail to teach or suggest such a feature.

Swenson relates to a circuit for implementing a multi-channel parallel to serial conversion and a multi-channel serial to parallel conversion in one minimal RAM matrix. In that regard, Swenson shows in Fig. 1, registers 1-8 for receiving multi-channel serial data, RAM 10 for receiving the multi-channel serial data from the registers, MUX 11 for reading the data stored in RAM 10, and registers 21-28 for providing the data from RAM 10 to parallel form.

In operation, the serial data is received from registers 1-8 and stored in RAM 10 in accordance with address 9 until the matrix is full (col. 3, lines 24-46). When it is desired to read the data, MUX 11 reads the data from RAM 10 and provides the read data to each of registers 21-28 in accordance with address 9, applied to selector 12, in order to generate a block of parallel data (col. 3, lines 47-64). In practice, all RAM 10 write operations are to a row of RAM 10 array, and all RAM 10 read operations are from a column of the RAM 10 array (col. 3, lines 64-67).

It is asserted that part 11 to parts 21-28 corresponds to the previously recited serial to parallel converter. Claim 1 has been amended to recite

> *a serial-to-parallel converter having a single serial data input line adapted to receive time-division multiplexed serial data from a plurality of data sources, and having a plurality of parallel output lines for* ***providing thereon a packet*** *of said time-division multiplexed serial data in parallel form* ***to one of a plurality of devices associated with data applications****;*

Swenson et al. shows registers 21-28 for providing serial to parallel output, but says nothing about providing the packet to one of a plurality of devices associated with data application. The cited portion of Swenson refers to each bit of the serial data, being transferred to RAM 10, rather than providing a packet of data to on e of the recited devices. Thus, Applicants submit that Swenson et al. fails to disclose a notable limitation of the amended claims.

It is also asserted that part 9 shown in Fig. 1 of Swenson corresponds to the previously recited enable logic. Claim 1 has been amended to recite

*enable logic coupled to each of said plurality of devices and adapted to provide at least one* ***data valid signal that identifies which of said plurality of devices is associated with a particular packet*** *of said time-division multiplexed serial data.*

Nowhere does Swenson disclose or suggest such a feature. As noted above, Swenson fails to disclose providing the packet to one of plurality of devices associated with data application. Since, Swenson is directed to providing a multi-channel serial to parallel converter with minimal number of elements, i.e., registers and RAM array, Swenson is not concerned with controlling the transfer of the parallel data to other devices associated with data application after it is output from the serial to parallel converter. Therefore, there is no mention of an enable logic that provides a data valid signal that identifies which of the plurality of devices is associated with a particular packet of the time-division multiplexed serial data.

The cited part 9 corresponds to the address applied to selector 12, which enables one of the registers 21-28 in sequence in order to load the data read from RAM 10 to the respective registers, to thereby enable the serial to parallel conversion. Thus, it is clear that **part 9 is part of the process of serial to parallel conversion**, and does not relate to providing a signal that identifies which of the devices is associated with a particular packet of the time-division multiplexed serial data.

In view of the above, Applicants submit that Swenson et al., fails to disclose or suggest notable limitation of the claimed invention, and thus, claims 1, and 6, and the claims that depend therefrom, are not anticipated by the teachings of Swenson, et al.

Having fully addressed the Examiner's rejections, Applicants submit that the present application is in condition for allowance and respectfully request such action. No further fee is believed due in regard to the present amendment. However, if a fee is due, please charge the fee to Deposit Account 07-0832. Should any questions arise regarding any of the above, the Examiner is requested to contact the undersigned at 609-734-6815.

Respectfully submitted,
T. Horlander, et al.

By: Paul P. Kiel
Attorney for Applicants
Registration No. 40,677

THOMSON Licensing Inc.
PO Box 5312
Princeton, NJ 08543-5312

Date: Feb. 17, 2004

CERTIFICATE OF MAILING

I hereby certify that this amendment is being deposited with the United States Postal Service as First Class Mail, postage prepaid, in an envelope addressed to], Commissioner for Patents, Alexandria, Virginia 22313-1450 on:

2/17/04
Date

Eliza Buchalczyk